REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-33 in the application. Previously, the Applicants amended Claims 1, 4-5, 9, 12, 15-16, 20, 23, 26-27 and 31, added Claims 34-36 and canceled Claims 8, 19 and 30 without prejudice or disclaimer.

Previously, the Examiner indicated that dependent Claims 9, 20 and 31 include allowable subject matter. In the present amendment, the Applicants have amended independent Claims 1, 12 and 23 with subject matter from dependent Claims 9, 20 and 31. Additionally, dependent Claims 16 and 20 have been amended. Accordingly, the Applicants believe pending Claims 1-7, 9-18, 20-29 and 31-36 are in condition for allowance.

I. Rejection of Claims 1-3, 10, 12-14, 21, 23-25 and 32 under 35 U.S.C. §103

Previously, the Examiner rejected Claims 1-3, 10, 12-14, 21, 23-25 and 32 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,552,619 to Shastri in view of U.S. Patent 6,018,547 to Arkhipkin, *et al.*, and in further view of U.S. Patent 5,651,031 to Ishizu. The Applicants respectfully disagree.

The Examiner recognized that Shastri does not teach or suggest a multi-channel serdes receiver with each receiver including integrators and latches configured to perform demultiplexing of a data signal received thereby. To teach demultiplexing using integrators and latches, the Examiner cited Arkhipkin. Arkhipkin discloses a PNS demodulator 264 that includes accumulators, switches and delays. (*See* column 2, lines 52-60 and Figures 2B and 2C.) The Examiner asserts that the accumulators and the latches of the PNS demodulator 264 correspond to the integrators and latches

of the presently claimed invention. As argued in previous responses, the Applicants respectfully disagree. Furthermore, even assuming *arguendo* that the Examiner's assertion is correct, the accumulators and the latches of Arkhipkin are not configured to perform a first demultiplexing of a data signal and a second demultiplexing of the data signal as recited in amended independent Claims 1, 12 and 23. For example, a second demultiplexing of an input signal is not provided. (*See* Figure 2c.) As such, Arkhipkin and Shastri, individually or in combination, do not teach or suggest a multi-channel serdes receiver with each receiver including integrators and latches, wherein the integrators are configured to perform a first demultiplexing of a data signal received by each of the receivers and the latches are configured to perform a second demultiplexing of the data signal as recited in amended independent Claims 1, 12 and 23.

Ishizu was not cited to teach demultiplexing using integrators and latches. Additionally, the Applicants do not find where Ishizu cures the above deficiency of Shastri and Arkhipkin. Ishizu discloses using integrators in a clock phase detector of the clock recovery circuits (*see* column 1, line 47 to column 2, line 10 and Figure 26), but does not teach or suggest employing integrators for a first demultiplexing of a data signal and latches for a second demultiplexing of the data signal. Thus, Ishizu does not teach or suggest integrators configured to perform a first demultiplexing of a data signal and latches configured to perform a second demultiplexing of the data signal as recited in amended independent Claims 1, 12 and 23.

The previously cited combination, therefore, of Shastri, Arkhipkin and Ishizu does not teach or suggest each element of amended independent Claims 1, 12 and 23. As such, the cited combination does not provide a *prima facie* case of obviousness of independent Claims 1, 12 and

23 and Claims dependent thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection and allow issuance of Claims 1-3, 10, 12-14, 21, 23-25 and 32.

II. Rejection of Claims 4-7, 11, 15-22, 26-29 and 33 under 35 U.S.C. §103

Previously, the Examiner rejected dependent Claims 4-7, 11, 15-22, 26-29 and 33 under 35 U.S.C. §103(a) as being unpatentable over Shastri in view of Arkhipkin, Ishizu and in further view of other references. The other references have not been cited to teach or suggest a plurality of channel-specific receivers configured to receive a data signal and include integrators configured to perform a first demultiplexing of the data signal and latches configured to perform a second demultiplexing of the data signal as recited in amended independent Claims 1, 12 and 23. Instead, these references have been cited to teach the subject matter of specific dependent claims listed above. Accordingly, the cited combination of Shastri, Arkhipkin and Ishizu with any of the other references does not teach or suggest each and every element of amended independent Claims 1, 12 and 23. As such, the cited combinations do not provide a *prima facie* case of obviousness of Claims 1, 12 and 23 and Claims dependent thereon. The cited combinations, therefore, do not render dependent Claims 4-7, 11, 15-22, 26-29 and 33 unpatentable and the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of dependent Claims 4-7, 11, 15-22, 26-29 and 33 and allow issuance thereof.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants submit that all of the Claims currently pending in this application are in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-7, 9-18, 20-29 and 31-36.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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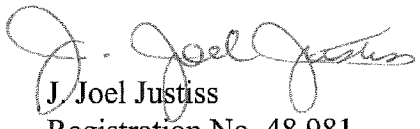

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